

REMARKS

The Applicants thank the Examiner for the careful examination of this application and respectfully request the entry of the amendments indicated hereinabove.

Claims 1-8 are pending; Claims 1, 3, and 5-8 are rejected and Claims 2 and 4 are objected to. Claims 1, 7, and 8 are amended hereinabove.

Independent Claim 1 positively recites depositing a first layer of copper grains having a first initial grain size over a copper seed layer, the first layer of copper grains being deposited by an electroplating process; and depositing a second layer of copper grains having a second initial grain size over the first layer of copper grains having the first initial grain size, the second layer of copper grains being deposited by an electroplating process. These advantageously claimed features are not taught or suggested by the patents granted to Park et al. and Uzoh et al., either alone or in combination.

Park et al. teaches away from the advantageously claimed invention by teaching the formation of a second Cu layer 130 over a first Cu layer 110 in which the copper grains of the first copper layer 100 were changed by the annealing process to form the first copper layer 110 (column 2 lines 36-38 and 64-66, column

3 lines 32-34, column 6 lines 12 and 33-35, FIGS. 5-6), but not the formation of a second layer of copper grains over a first layer of copper grains still having the first initial grain size (that have not been modified by the annealing process – i.e. Park et al.'s element 100), which is advantageously claimed. This is because Park et al. teaches an annealing step that is a "necessary" treatment following the deposition of the first layer of Cu grains (column 4 lines 32-34 and 45-47, column 5 lines 49-54, see also column 2 lines 34-35 and 61-65 and column 3 lines 29-31). In summary, Park et al. teaches away from the advantageously claimed invention because Park et al. states that an annealing step between the deposition of the first and second layer of copper film is a "necessary" step after the deposition of the first electroplating film and before the deposition of the second copper film in order to "form a stable and generally void-free structure that, after annealing, is compatible with a subsequent thicker (large-grained) Cu layer created in a next cavity-filling deposition process" (column 4 lines 36-39, see also column 5 lines 50-54). Moreover, Park et al. teaches that the grain size of the first layer is increased before the deposition of the second layer of copper (column 5 lines 50-51). The Applicants submit that the advantageously claimed process - whereby there is no anneal step between the formation of the first and second layer of copper grains - avoids the problem of the unwanted insulating copper oxide film that is noted in Park et al. (column 6 lines 14-18).

Like Park et al., Uzoh et al. teaches away from the advantageously claimed invention by also teaching that the first conductive layer is modified (by planarization and annealing) before the formation of the second conductive layer (column 4 lines 25-34 and 62-67, column 5 lines 1-35), but not the formation of a second layer of copper grains over a first layer of copper grains having the first initial grain size as is advantageously claimed. As stated in column 1 lines 35-36, annealing promotes grain growth. The planarization process also modifies the grain size of the first conductive layer (column 5 lines 35-67, column 6 lines 1-28).

Furthermore, the Applicants submit that one skilled in the art would not combine the teachings of an interconnect fabrication process using conforming layers (Park et al., FIG. 8, column 6 lines 31-35) with an interconnect fabrication process using planar layers (Uzoh et al., FIG. 8c, column 6 lines 42-44 and 58-59). In addition, the Applicants note that Park et al. teaches away from a planarization step following the formation of the first conductive layer (column 6 lines 37-38) as taught by Uzoh et al. (column 4 lines 40-44). Moreover, the Applicants submit that one skilled in the art would not combine a process that teaches an anneal after the formation of the second conductive layer (Uzoh et al., column 7 lines 49-50) with a that teaches away from the use of an anneal step after the deposition of the second metal film (Park et al., column 2 lines 38-39 and 66-67, column 3 lines 34-36).

Therefore, the Applicants respectfully traverse the Examiner's rejection of Claim 1 and respectfully assert that Claim 1 is patentable over the patents granted to Park et al. and Uzoh et al. Furthermore, Claims 2-6 are allowable for depending on allowable independent Claim 1 and, in combination, including limitations not taught or described in the references of record.

Independent Claim 7 positively recites depositing at least one additional layer of copper grains of differing initial grain sizes over the first layer of copper grains having the first initial grain size, the at least one additional layer of copper grains being deposited by an electroplating process. These advantageously claimed features are not taught or suggested by the patent granted to Park et al.

Park et al. teaches away from the advantageously claimed invention by teaching the formation of a second Cu layer 130 over a first Cu layer 110 in which the copper grains of the first copper layer 100 were changed by the annealing process to form the first copper layer 110 having increased grain size (column 2 lines 36-38 and 64-66, column 3 lines 32-34, column 5 lines 50-51, column 6 lines 12 and 33-35, FIGS. 5-6), but not the formation of a second layer of copper grains over a first layer of copper grains that are still the first initial grain size (i.e. that have not been modified by the annealing process), which is advantageously claimed. This is because Park et al. teaches an annealing step that is a "necessary" treatment following the deposition of the first layer of Cu grains

(column 4 lines 32-34 and 45-47, column 5 lines 49-54, see also column 2 lines 34-35 and 61-65 and column 3 lines 29-31). In summary, Park et al. teaches away from the advantageously claimed invention because Park et al. states that an annealing step between the deposition of the first and second layer of copper film - which increases the grain size of the first copper film - is a "necessary" step after the deposition of the first electroplating film and before the deposition of the second copper film (column 4 lines 36-39, see also column 5 lines 50-54).

Therefore, the Applicants respectfully traverse the Examiner's rejection of Claim 7 and respectfully assert that Claim 7 is patentable over the patent granted to Park et al.

Independent Claim 8 positively recites depositing a second layer of copper grains having a second initial grain size over the first layer of copper grains having the first initial grain size. In addition, Claim 8 positively recites the step of annealing the semiconductor wafer after the step of depositing the second layer of copper grains. These advantageously claimed features are not taught or suggested by the patent granted to Park et al.

Park et al. teaches away from the advantageously claimed invention by teaching the formation of a second Cu layer 130 over a first Cu layer 110 in which the copper grains of the first copper layer 100 were changed by the annealing

process to form the first copper layer 110 having increased grain size (column 2 lines 36-38 and 64-66, column 3 lines 32-34, column 6 lines 12 and 33-35, FIGS. 5-6), but not the formation of a second layer of copper grains over a first layer of copper grains that are still the first initial grain size (that have not been modified by the annealing process), which is advantageously claimed. This is because Park et al. teaches an annealing step that is a "necessary" treatment following the deposition of the first layer of Cu grains (column 4 lines 32-34 and 45-47, column 5 lines 49-54, see also column 2 lines 34-35 and 61-65 and column 3 lines 29-31). In summary, Park et al. teaches away from the advantageously claimed invention because Park et al. states that an annealing step between the deposition of the first and second layer of copper film – which increases the grain size of the first copper film - is a "necessary" step after the deposition of the first electroplating film and before the deposition of the second copper film (column 4 lines 36-39, see also column 5 lines 50-54).


The Applicants respectfully traverse the assertion in the Office Action (page 4 that Park et al. teaches - in column 5 lines 49-50 - the step of annealing the semiconductor wafer after the deposition of the second metal film. The Applicants submit that Park et al. only teaches the use of an anneal step after the deposition of the first metal film (column 2 lines 35-36 and 62-64, column 3 lines 29-33, column 4 lines 36-37, column 5 lines 49-51). Furthermore, the Applicants submit

that Park et al. teaches away from the use of an anneal step after the deposition of the second metal film (column 2 lines 38-39 and 66-67, column 3 lines 34-36).

Therefore, the Applicants respectfully traverse the Examiner's rejection of Claim 8 and respectfully assert that Claim 8 is patentable over the patent granted to Park et al.

For the reasons stated above, this application is believed to be in condition for allowance. Reexamination and reconsideration is requested.

Respectfully submitted,



Rose Alyssa Keagy
Attorney for Applicants
Reg. No. 35,095

Texas Instruments Incorporated
PO BOX 655474, M/S 3999
Dallas, TX 75265
Telephone: 972/917-4167
FAX: 972/917-4409/4418